Amendments to the Specification:

Please replace paragraph **[0010]** with the following amended paragraph:

[0010] According to one embodiment, the output signal representing the counter value is supplied to a partial comparator, which establishes threshold values for the counter value. These threshold values are in turn supplied to an expanded comparator, which produces multiple comparator output signals. The comparator output signals operate to enable an associated delay element, thereby controlling the speed ~~sped~~ with which the clock signal propagates through the delay line element. The expanded comparator preferably comprises a plurality of identical logical units, with a particular logic unit associated with each comparator output. The logic units couple to different threshold values from the partial comparator to define the state of each of the comparator outputs. The delay line preferably comprises a plurality of parallel transistor stacks that are selectively enabled by the output signals from the logical units in the expanded comparator. As each transistor stack is enabled, the speed with which the clock signal propagates through the delay line increases. Each of the transistor stacks preferably has different size transistors to provide a constant delay through each stack.

Please replace paragraph **[0034]** with the following amended paragraph:

[0034] The drain terminals of transistors 163, 167 comprise the CMP*n*_H output terminal. The data present on the CMP*n*_H output terminal preferably is latched by the high data latch 170. The high data latch 170 preferably comprises a pair of inverters 171, 173 constructed in conventional fashion as a data latch. As shown in Figure 4, the output terminal of inverter 173 connects to the input terminal of inverter 171. The output terminal of inverter 171 connects to the input terminal of inverter 173. In this fashion, the state value at the drain of transistors is reinforced and maintained in latch 170. Similarly, the drain terminals of transistors 153, 157 comprise the CMP*n*_L output terminal. This value preferably is latched by the low data latch 180. The low data latch 180 preferably comprises a pair of inverters 181, 183 constructed in conventional fashion as a data latch. As shown in Figure 4, the output terminal of inverter 183 connects to the input

terminal of inverter 181. The output terminal of inverter 181 connects to the input terminal of inverter 183. The net effect of the configuration shown in Figure 4 is that the output of OR gate 135 will be driven strongly by the high pass gate 165 when the clock signal (CLK) is high, and appear at the CMP*n*_H output terminal. Similarly, the inverted state of the OR gate output signal will be driven strongly by ~~be~~ the low pass gate 155. The output of the OR gate 135 will be asserted when the count value is equal to *n*, where *n* represents the particular logical unit that produces CMP*n*_H and CMP*n*_L. Thus, if the logical unit generates CMP5, then OR gate 135 will be asserted high when the count is 5 in the counter 50. This will cause the partial comparator to assert GTE1, GTE2, GTE3, GTE4, and de-assert GTE8 and GTE12. Because GTE4 and GTE1 are asserted, the output of AND gate 130 will be asserted, which will cause OR gate 135 to assert. This will cause CMP5_H to go high (*i.e.*, produce a "1" output) and CMP5_L to go low (*i.e.*, produce a "0" output) when the clock signal is high.